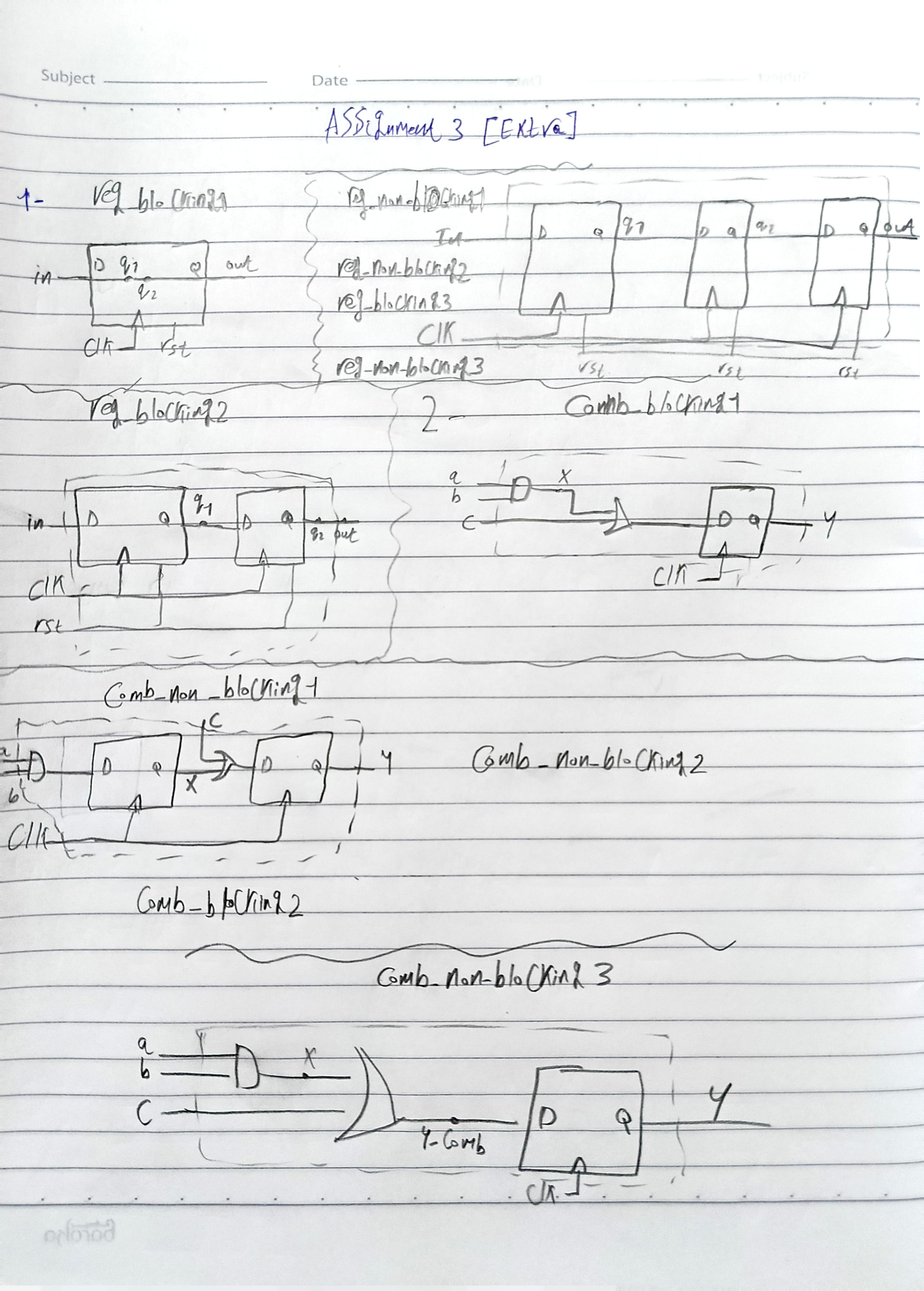
Digital Design Diploma

# **Assignment 3 (Extra)**

# **Sequential Logic Design**

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| **Group** | G2 |

**Submitted to: Eng. Kareem Waseem**

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**2) 4-bit synchronous counter with asynchronous active low set:**

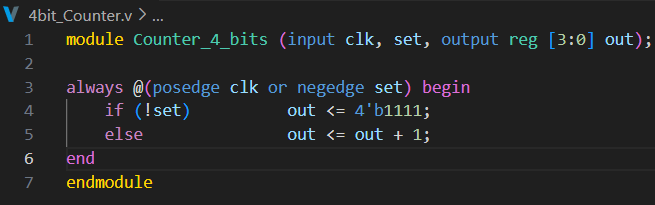
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Figure1: Q2 Code

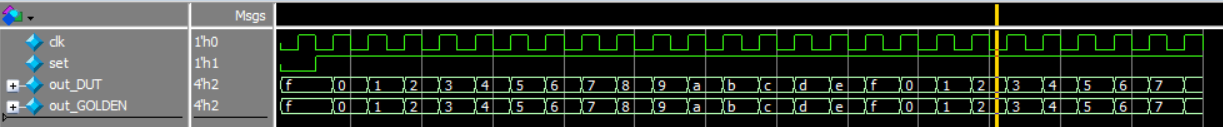
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Figure2: Q2 Wave

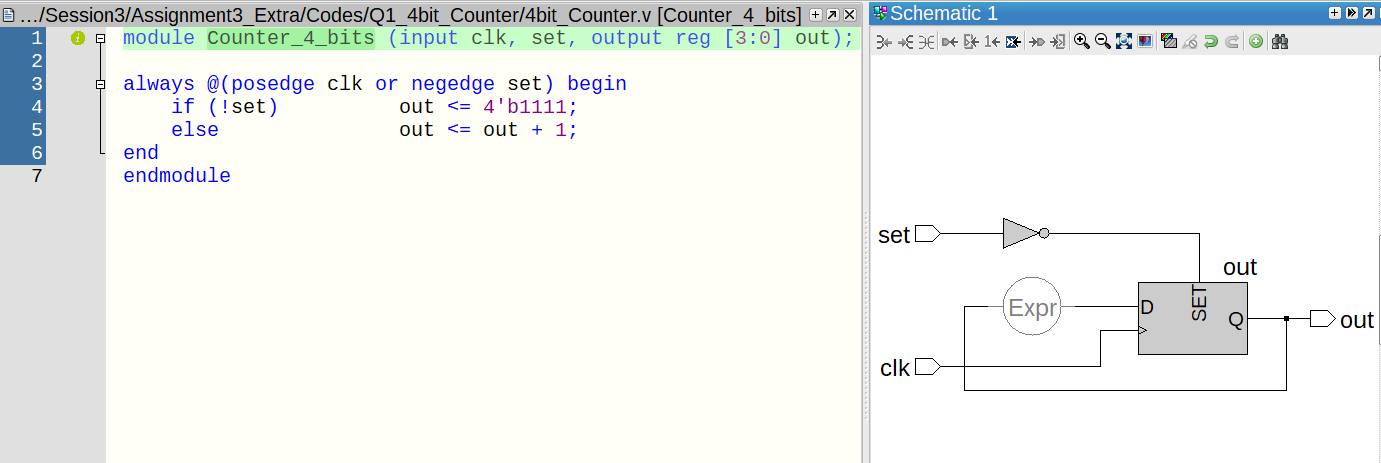
****

Figure3: Q2 Lint

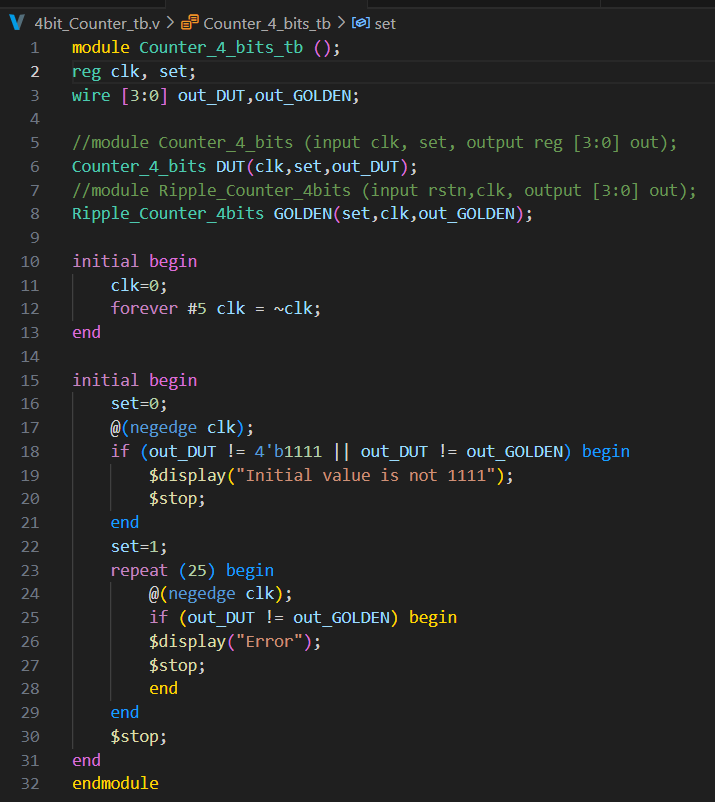
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Figure4: Q2 Testbench

**3) Extended Counter:**

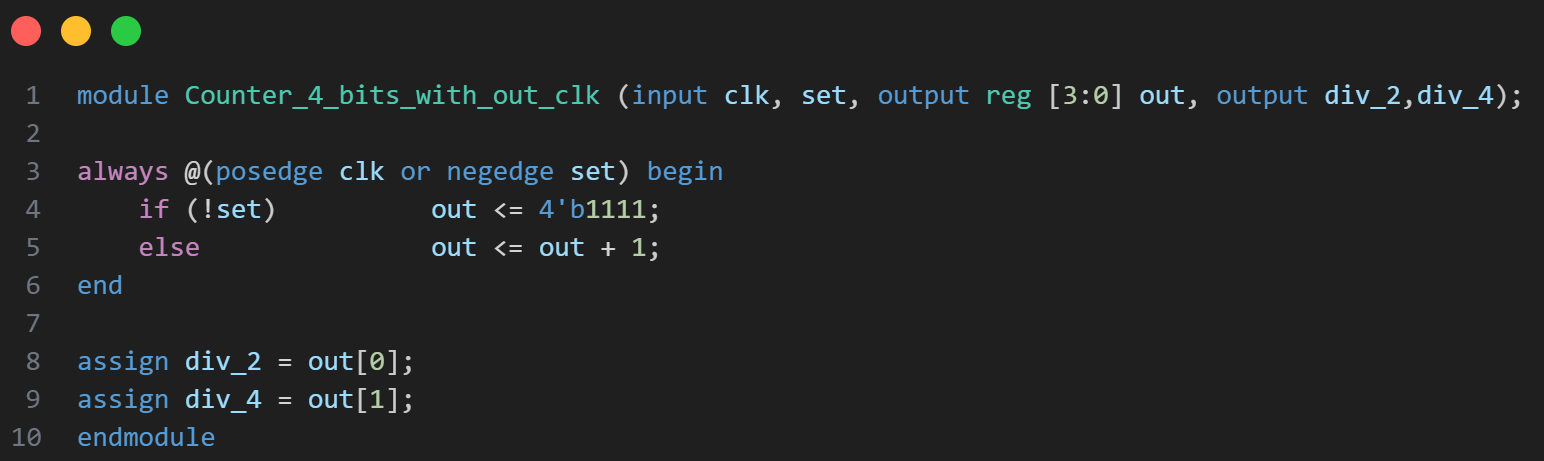
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Figure5: Q3 Code

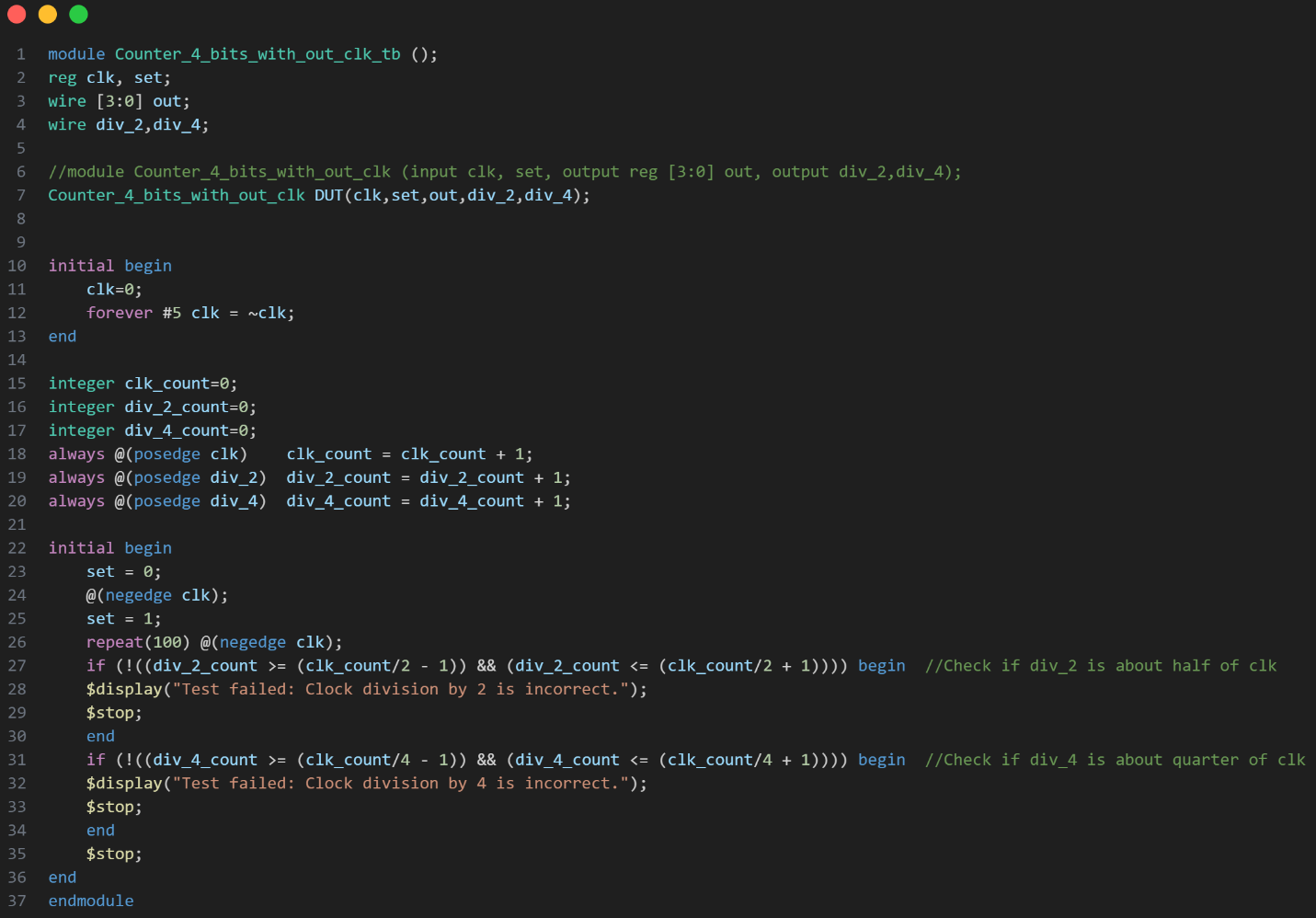
****

Figure6: Q3 Testbench

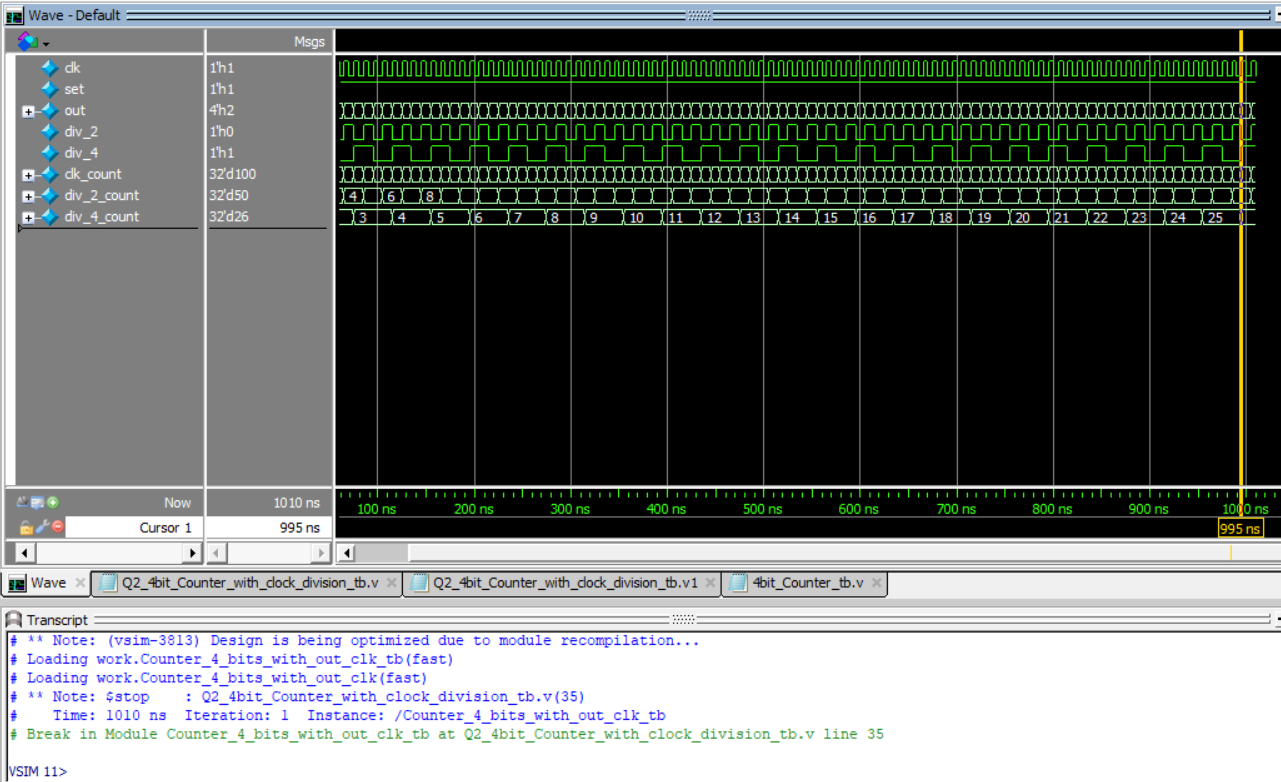
****

Figure7: Q3 Wave

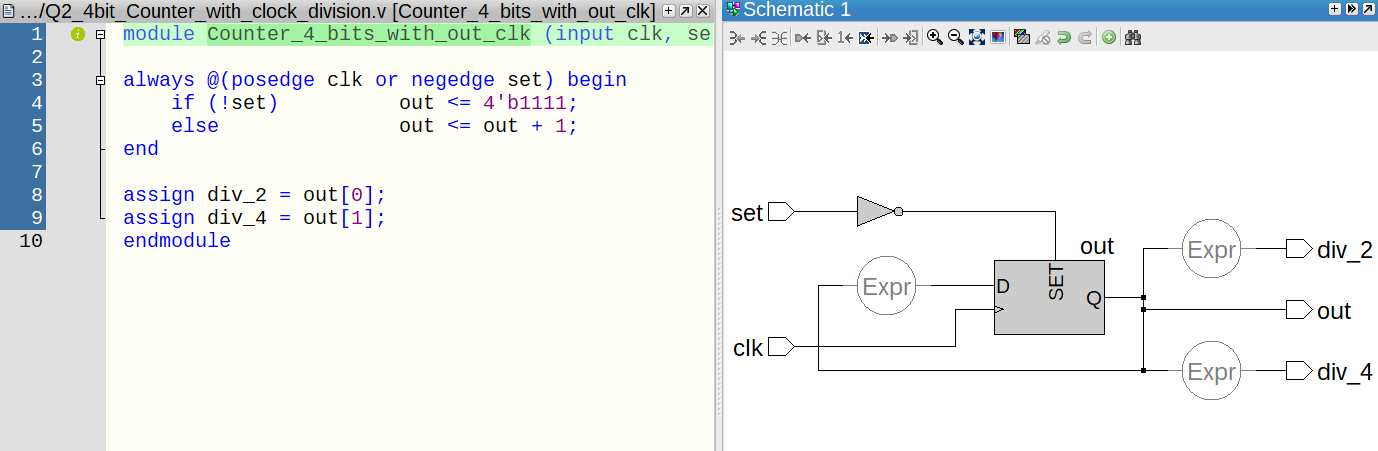
****

Figure8: Q3 Lint

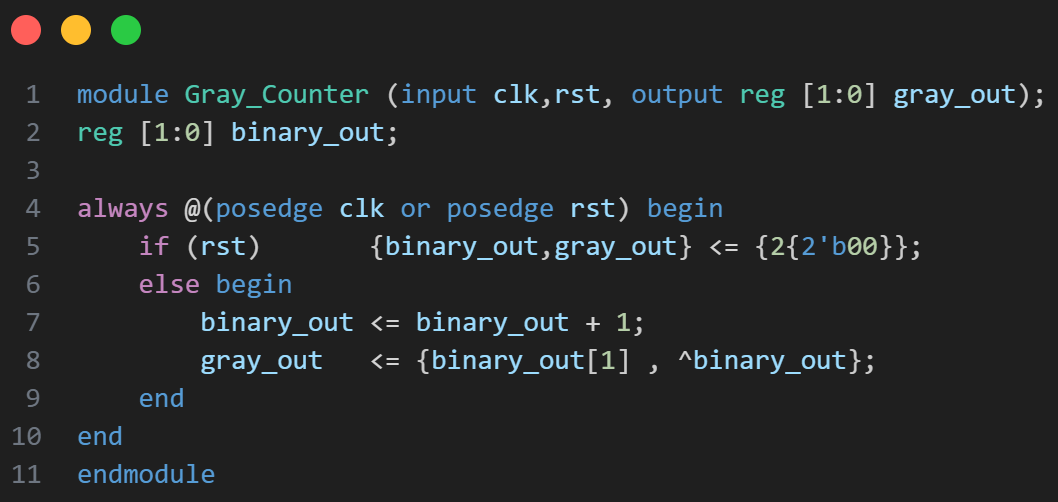
**4) Gray Counter:**

Figure9: Q4 Code

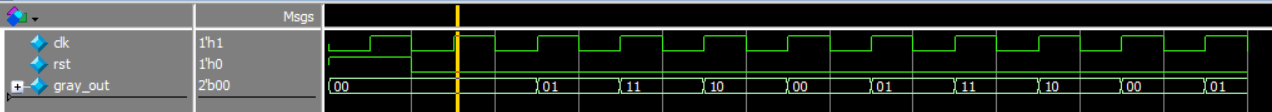
****

Figure10: Q4 Wave

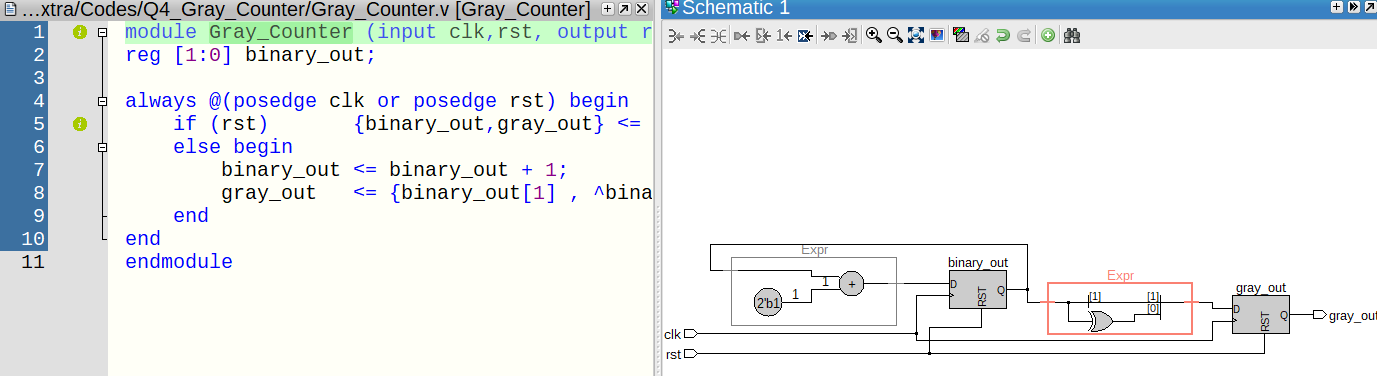
****

Figure11: Q4 Lint

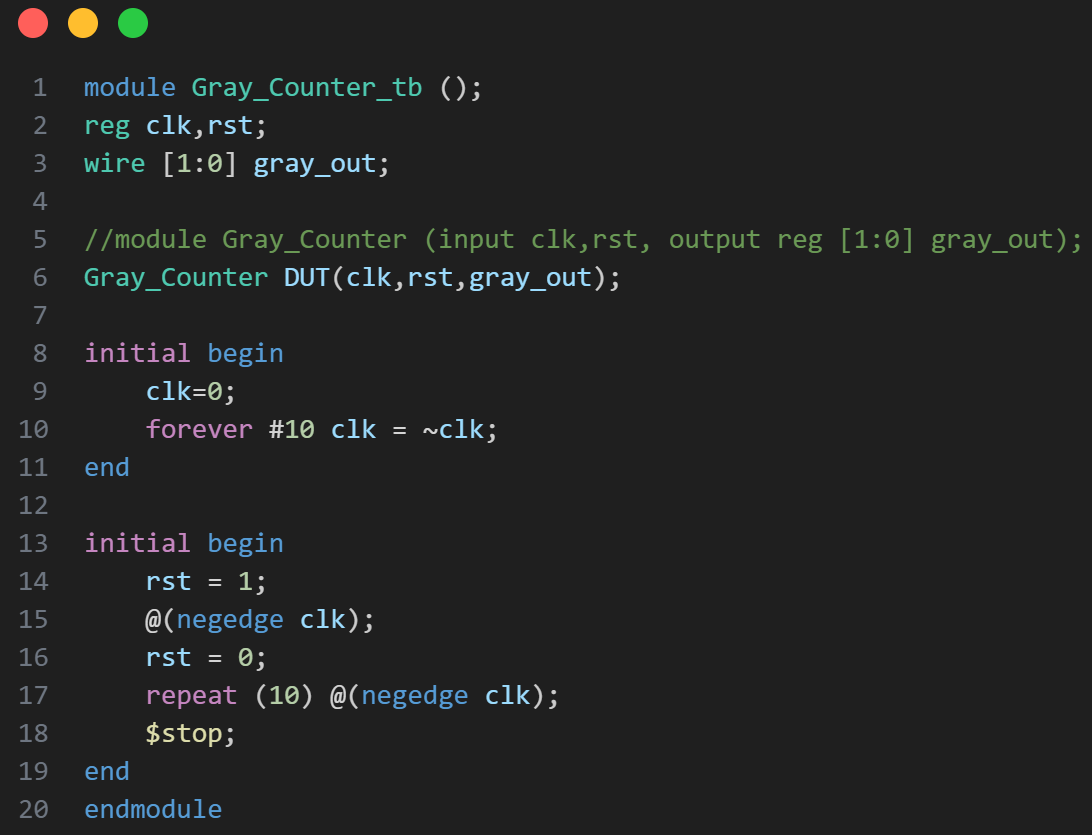
****

Figure12: Q4 Testbench